The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES S. BLOMGREN and FRITZ A. BOEHM

Appeal No. 2004-1094
Application No. 09/405,618

ON BRIEF

Before HAIRSTON, RUGGIERO, and DIXON, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-3, 6-8, 11-13, 16-18, and 21-23, which are all of the claims pending in this application.

We REVERSE.

Appellants' invention relates to a software modeling of logic signals capable of holding more than two values. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A signal model used in an N-NARY logic simulation, comprising:

a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

The prior art of record relied upon by the examiner in rejecting the appealed claims is as follows:

Giramma	5,706,476	Jan. 06, 1998
Leight et al. (Leight)	6,289,497	Sep. 11, 2001 (filed Dec. 11, 1998)

IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164), pp. i-iv and 1-17, approved Mar. 18, 1993.

Rozon, "On the Use of VHDL as a Multi-Valued Logic Simulator, **IEEE**, pp. 110-115 (1996).[1]

[1] The examiner has withdrawn his rejection over Rozon in the answer.

Claims 1-3, 6-8, 11-13, 16-18, and 21-23 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-35 of Leight. Claims 1-3, 6-8, 11-13, 16-18, and 21-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Giramma. Claims 1-3, 6-8, 11-13, 16-18, and 21-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Std_logic_1164.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed Aug. 27, 2003) for the examiner's reasoning in support of the rejections, and to appellants' brief (Paper No. 11, filed Jun. 4, 2003) and reply brief (Paper No. 13, filed Oct. 27, 2003) for appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we make the determinations which follow.

OBVIOUS-TYPE DOUBLE PATENTING

Appellants argue that at pages 29-34 of the brief that the claims of the instant application are not an obvious variation of the claims in the Leight patent. We agree with

appellants and further do not find that the examiner has made the requisite analysis of both sets of claims and the difference therebetween for a proper rejection under obvious-type double patenting. Therefore, we will not sustain the rejection under obvious-type double patenting.

ANTICIPATION

Appellants argue that the examiner has never developed an understanding of the substantial differences between the nonbinary technology and its modeling and the well-known extended-state modeling techniques applicable to binary logic. (Brief at pages 7-8.) The examiner maintains that the claim language does not reference the term FAST 14 and the claims are not drafted in terms of "means for" and that appellants are trying to read limitations from the specification into the claims. (Answer at page 7.) We disagree with the examiner and find that appellants have specifically defined the terms "N-NARY logic," "nonbinary," and "1-of-N logic signal" in appellants' specification and by incorporation by reference to other N-NARY logic patents so as to specifically define these terms. Therefore, we find it unreasonable for the examiner to interpret these terms in a manner inconsistent with appellants' specific definition or to require appellants to draft the claims in a "means plus function" format. The examiner then states that "if the current claim language contained limitations, as referred to by the Appellant[s] in the specification, then the claims would be allowable." (Answer at page 8.) We find that the instant claim

language does contain these limitations and agree with the examiner's conditional statement. Therefore, we will not sustain the examiner rejection of independent claims 1, 6, 11, 16, and 21 and their respective dependent claims since the examiner has not established a ***prima facie*** case of anticipation.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-3, 6-8, 11-13, 16-18, and 21-23 under obviousness-type double patenting and under 35 U.S.C. § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

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JDL/vsh

BOOTH & WRIGHT LLP
P. O. BOX 50010
AUSTIN, TX 78763-0010